GIGALIGHT 100G QSFP28 SR2 Optical Transceiver
P/N: GQS-MPO101-SR2C

Features

✓ QSFP28 module form factor

✓ Support QSFP28 SFF-8436/8636

✓ 2x53.125Gbps(26.5625GBd) PAM4 parallel optics architecture

✓ 4x25.78125Gbps NRZ retimed electrical I/O

✓ 2 channels 850nm VCSEL Array and PIN photo detector array

✓ Internal 4:2 Gearbox with KP4 FEC circuits on both receiver and transmitter channels

✓ Single MPO12/APC receptacle(Only use channel 1 and channel 2)

✓ Maximum link length of 100m OM4,70m OM3 (DSP KP4-FEC is ON)

✓ Built-in digital diagnostic functions

✓ Operating case temperature range: 0 to 70°C

✓ Single 3.3V power supply

✓ Low power consumption < 4W

✓ RoHS compliant (lead free)

Applications

✓ 100G SR2（2x 50G PAM4） applications

✓ High-speed interconnects within and between switches, routers and transport equipment

✓ Server-server clusters, super-computing interconnections

✓ Proprietary backplanes

✓ Interconnects rack-to-rack, shelf-to-shelf, board-to-board, board-to-optical backplane

Description

The Gigalight 100G SR2 QSFP28 optical transceiver is designed for using in 100-Gigabit Ethernet links up to 70m using OM3 and 100m using OM4. It is compliant with the QSFP28 MSA, IEEE 802.3cd and CAUI-4(no FEC)[1]. Digital diagnostics functions are available via the I2C interface, as specified by the QSFP28 MSA. The module incorporates 2 channels 850nm VCSEL Array and PIN photo detector array. This results in an aggregate bandwidth of 100Gbps into a MPO cable. This module can convert 4 channels of 25Gbps (NRZ) electrical input data to 2 channels of 50Gbps (PAM4) optical signal, and also can convert 2 channels of 50Gbps

(PAM4) optical signal to 4 channels of 25Gbps (NRZ) electrical output data. The electrical interface uses a 38-contact edge type connector. This transceiver is a high performance module for short-range duplex data communication and interconnects applications.

Note:
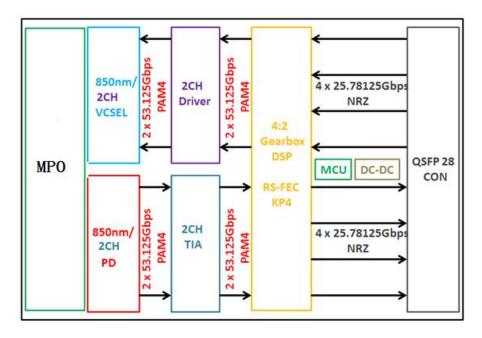
1. KR-FEC is optional, please contact us if necessary.

Figure 1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.3	3.6	V
Input Voltage	V_{in}	-0.3	Vcc+0.3	V
Storage Temperature	T_s	-20	85	ºC
Case Operating Temperature	T_c	0	70	ºC
Humidity (non-condensing)	Rh	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Operating Case temperature	T_c	0	-	70	ºC

Signal Rate per Electrical Channel (4 x 25G)		-	25.78125	-	Gbps
Signal Rate per Optical Channel (2 x 50G)		-	53.125	-	Gbps
Humidity	Rh	5	-	85	%
Power Dissipation	P_m	-	-	4	W
Fiber Length for OM3		-	-	70	m
Fiber Length for OM3		-	-	100	m

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude[1]	ΔV_{in}	-	-	1200	mVp-p
Differential Output Voltage Amplitude[2]	ΔV_{out}	-	-	1200	mVp-p

Note:

1. Differential input voltage amplitude is measured between TxnP and TxnN.

2. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter					
Center Wavelength	λc	840	850	860	nm
RMS Spectral Width	Δλ			0.6	nm
Average Launch Power (each lane)	P_{out}	-6.5		4	dBm
Outer Optical Modulation Amplitude (each lane)	OMA_{out}	-4.5		3	dBm
Launch power in OMA_{outer} minus TDECQ	P_{tdecq}	-5.9			dBm
Transmitter and dispersion eye closure (each	TDEC			4.5	dB
Average launch power of off transmitter(each	P_{off}			-30	dBm
Outer Extinction Ratio	ER	3			dB
Optical Return Loss Tolerance	ORLT			12	dB
Receiver					
Center Wavelength	$λ_c$	840	850	860	nm
Damage threshold	Rdam			4	dBm
Average Receive Power (each lane)	Pin	-7.9		4	dBm
Receiver Power (OMA_{outer}) (each lane)	OMA_{out}			3	dBm
Receiver reflectance	Pref			-12	dB
Stressed Receiver Sensitivity (OMA_{outer}) (each lane)	Sens			-3	dBm
Receiver Sensitivity (OMA_{outer}) (each lane) [Note1]	Sen			-7	dBm

			-10	dBm
LOS Assert			-10	dBm
LOS De-Assert			-8.5	dBm
LOS Hysteresis		0.5		dB

Note:

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FECs

Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground[1]
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground[1]
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground[1]
8	LVTTL-I	MODSEIL	Module Select[2]
9	LVTTL-I	ResetL	Module Reset[2]
10		VCCRx	+3.3V Receiver Power Supply
11	LVCMOS-I	SCL	2-wire Serial interface clock[2]
12	LVCMOS-I/O	SDA	2-wire Serial interface data[2]
13		GND	Module Ground[1]
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module Ground[1]
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output
19		GND	Module Ground[1]
20		GND	Module Ground[1]
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground[1]
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground[1]

27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board[2]
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power Mode[2]
32		GND	Module Ground[1]
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground[1]
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground[1]

Note:

1. Module circuit ground is isolated from module chassis ground within the module.

2. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

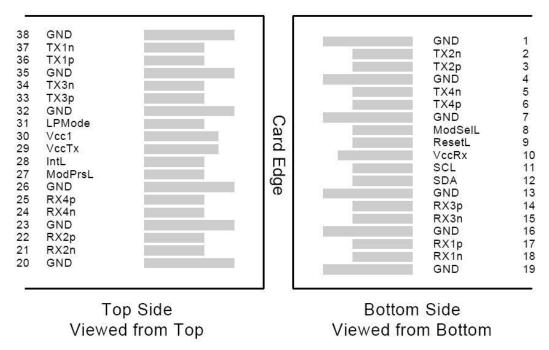*Figure 2. Electrical Pin-out Details*

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Gigalight QSFP28 modules operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

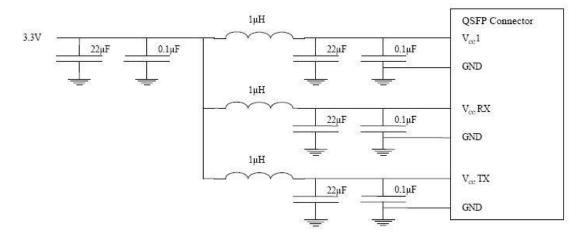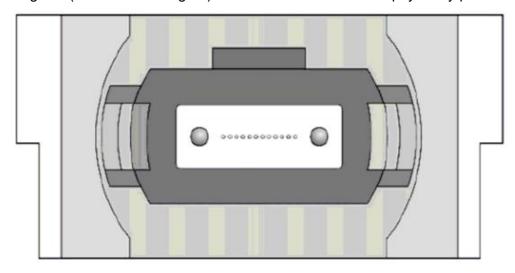The host board should use the power supply filtering shown in Figure 3.

Figure 3. Host Board Power Supply Filtering

Optical Interface Lanes and Assignment

The optical interface port is a male MPO connector.The four fiber positions on the left as shown in Figure 4, with

the key up, are used for the optical transmit signals (Channel 1 through 2). The fiber positions on the right are used for the optical receive signals (Channel 2 through 1). The central four fibers are physically present.

Transmit Channels: 1 2
Unused positions: x x x x
Receive Channels: 2 1

Figure 4. Optical Receptacle and Channel Orientation

DIAGNOSTIC MONITORING INTERFACE (OPTIONAL)

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	+3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Digital diagnostics monitoring function is available on all Gigalight QSFP28 transceivers. A 2-wire serial interface provides user to contact with module.

The structure of the memory is shown in Figure 4. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.
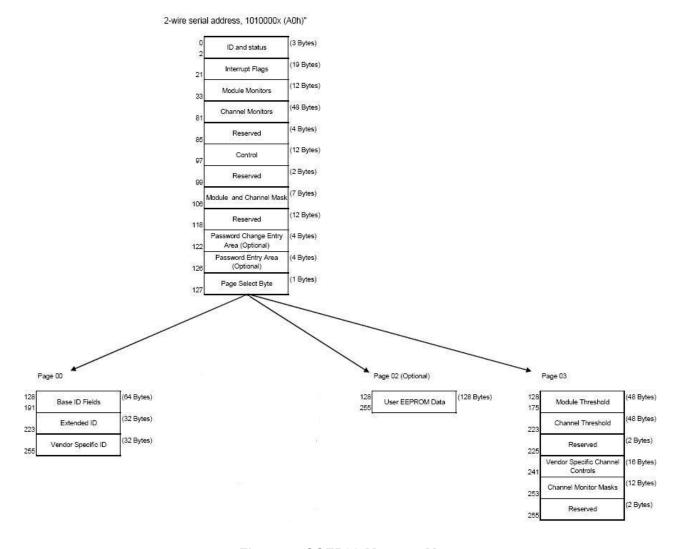

Figure 5. QSFP28 Memory Map

Byte Address	Description	Type
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Reserved (4 Bytes)	Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Figure 6. Low Memory Map

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure 7. Page 03 Memory Map

Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mbits/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 μm (1 Byte)	Link length supported for EBW 50/125 μm fiber, units of 2 m
144	Length 50 μm (1 Byte)	Link length supported for 50/125 μm fiber, units of 1 m
145	Length 62.5 μm (1 Byte)	Link length supported for 62.5/125μm fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand[†]
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tol. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

Figure 8. Page 00 Memory Map

Page02 is User EEPROM and its format decided by user.

The detail description of low memory and Page 00. Page 03 upper memory please see SFF-8436 document.
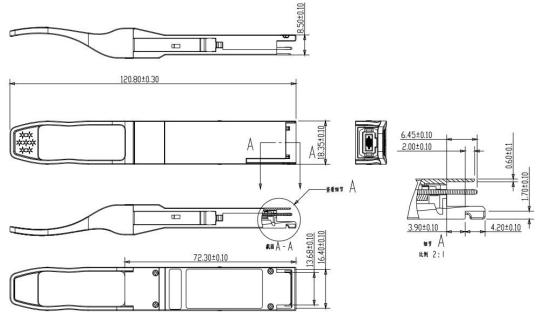
Mechanical Dimensions(Unit:mm)

Figure 9. Mechanical Specifications

Regulatory Compliance

Gigalight GQS-MPO101-SR2 transceivers are Class 1 Laser Products. They meet the requirements of the following standards.

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. QSFP28 MSA
2. SFF-8436 QSFP+

3. IEEE802.3cd 200GBASE-SR4

Ordering Information

Part Number	Product Description
GQS-MPO101-SR2	100G QSFP28 SR2(2x50G PAM) 850nm, OM3 70m, OM4 100m, MMF, MPO12/APC

⚠️CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

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Revision History

Revision	Date	Description
V0	Dec.-1-2025	Advance Release.